



UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/665,415 09/20/00 NAKAGAWA

K 500-0-240

EXAMINER

MM91/1105

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WASHINGTON DC 20005-3096

~~PAPER NO.~~

ART UNIT

PAPER NUMBER

2811
DATE MAILED:

11/05/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.
09/665,415

Applicant(s)
Nakagama et al

Examiner
Nitin Parekh

Art Unit
2811



-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on Sep 20, 2001
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 35 C.D. 11; 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3 is/are pending in the application.
- 4a) Of the above, claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claims _____ are subject to restriction and/or election requirements.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

- 13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
- a) ☒ All b) ☐ Some* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- *See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

- 15) ☒ Notice of References Cited (PTO-892) 18) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 19) ☐ Notice of Informal Patent Application (PTO-152)
- 17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____ 20) ☐ Other: _____

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DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (APA) in view of Amagai (US Pat. 6144102) and Jiang et al (US Pat. 6048755).

Regarding claims 1 and 2, the APA (Fig. 4 and 5) discloses a semiconductor device comprising:

- a semiconductor element having a primary surface with an element electrode and a back surface
- a circuit board having a primary surface and a back surface with a board electrode, the circuit board having predetermined opening hole
- the primary surface of the element being bonded to the primary surface of the circuit board by means of an adhesive layer
- the element electrode of the semiconductor element being connected to the board electrode provided on the back surface of the board via the opening hole, and

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- the surrounding regions of the side surfaces of the semiconductor element on the circuit board being sealed with a resin so as to assume a flange structure/shape.

The APA discloses bonding the primary surface of the element with the primary surface of the circuit board by means of an adhesive layer which is of the same size as that of the primary surface of the element but fails to specify using an adhesive layer which is of greater size than that of the primary surface of the element.

Amagai teaches using an adhesive layer (8 in Fig. 7) which is of greater size than that of the primary surface of the element (1 in Fig. 7) to improve rigidity and to reduce stress in a chip size package (Col. 6, line 25-45).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate an adhesive layer which is of greater size than that of the primary surface of the element to improve rigidity and to reduce stress using Amagai's device structure in the APA.

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Regarding claim 3, the APA fails to specify sealing the back surface of the semiconductor element on the circuit board with a resin.

It is conventional in the chip packaging and encapsulation technology art to encapsulate/seal all exposed surfaces of the semiconductor element to provide added protection for the device. Jiang et al teach using a conventional sealing resin/mold (38 in Fig. 1A) surrounding the side surfaces and the back surface of the semiconductor element to provide added protection/sealing for the device (Col. 1).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a resin sealing the side surfaces and the back surface of the semiconductor element on the circuit board to provide added protection/sealing, improve rigidity and to reduce stress using Amagai and Jiang et al's structures in the APA.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

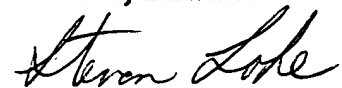
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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

11-01-01

Steven Loke
Primary Examiner

A handwritten signature in cursive script, appearing to read "Steven Loke", written in black ink.